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Electronics COOLING

SEPTEMBER 2013
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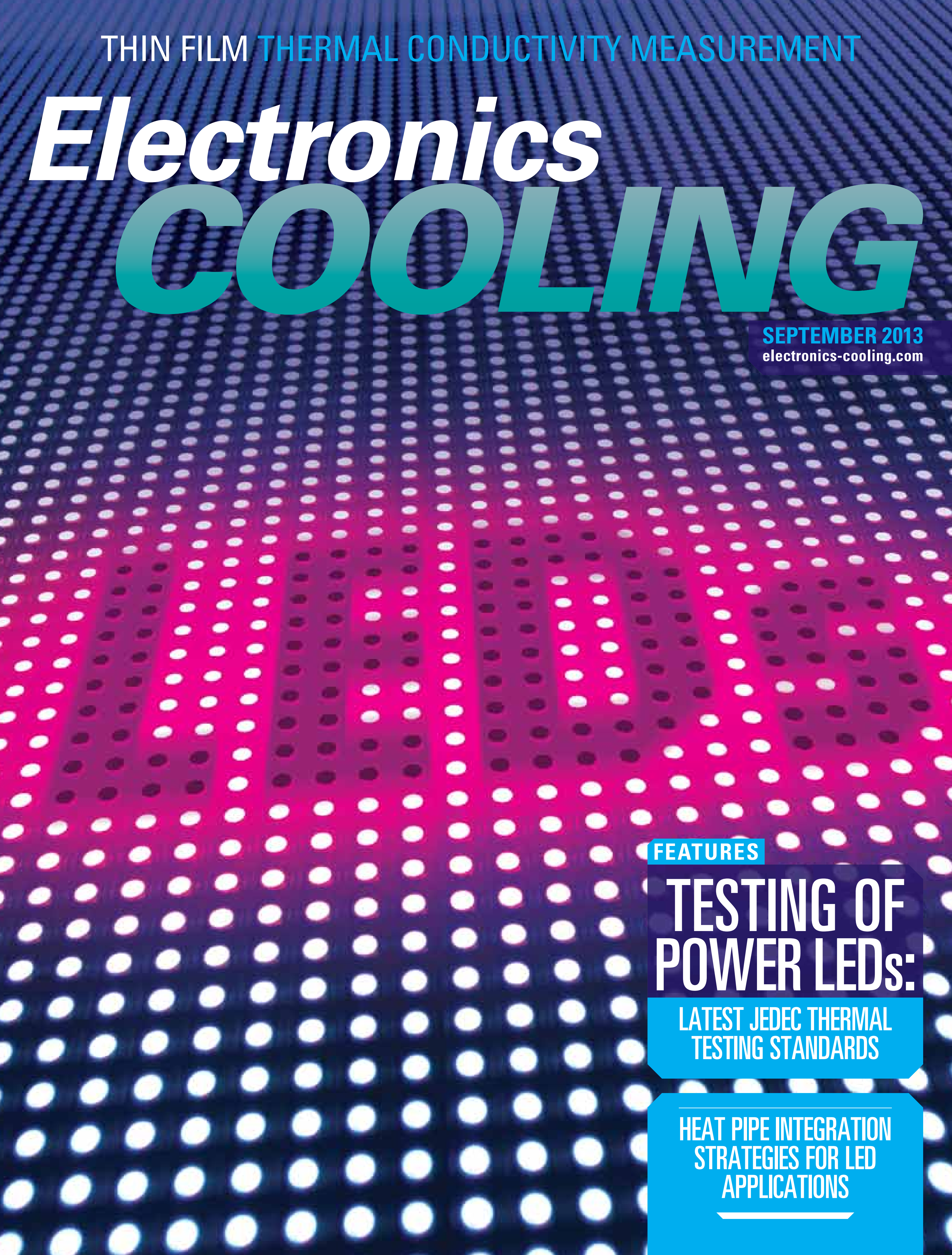

FEATURES

TESTING OF POWER LEDs:

LATEST JEDEC THERMAL TESTING STANDARDS

HEAT PIPE INTEGRATION STRATEGIES FOR LED APPLICATIONS

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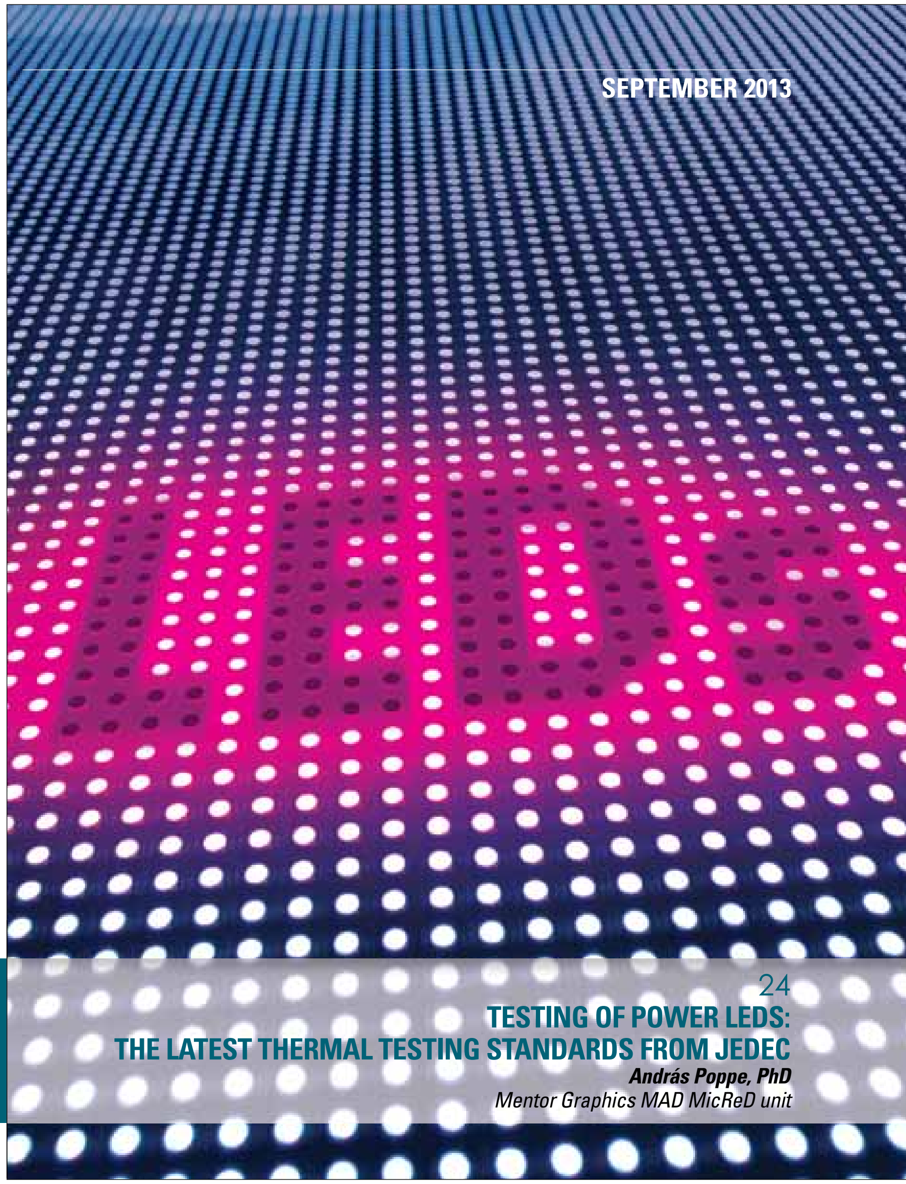

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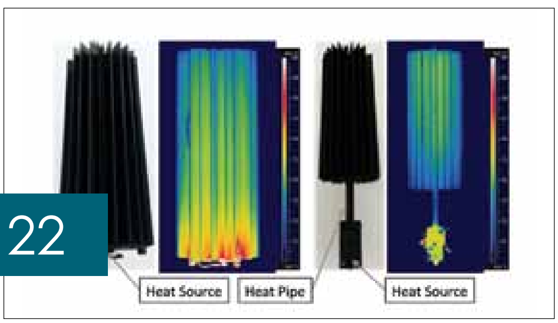

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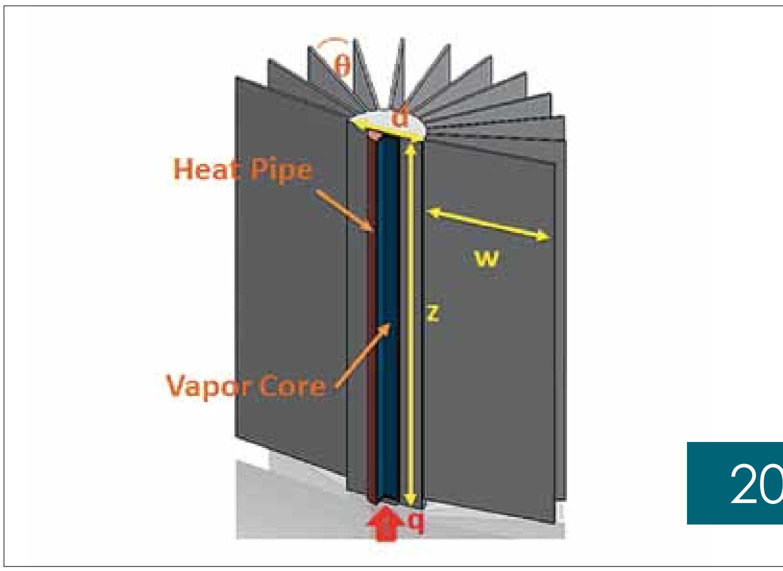

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Editorial

Getting Back to Basics

Peter Rodgers, Editor-in-Chief, September 2013

AS A YOUNG ENGINEER in the 1990s, I considered Electronics Cooling magazine as one of the first ports of call as a reference source when venturing into a new area of electronics thermal design. When I was invited to join Electronics Cooling's editorial team, I re-read the first editorial by Kaveh Azar [1]. He outlined the need at that time (1995) for a publication vehicle that could assemble, focus and disseminate pertinent practical information related to electronics cooling. Emphasis was placed on the word "practical," to ensure that Electronics Cooling would serve as a source of useful information to the thermal community. Eighteen years later, there is little doubt that Electronics Cooling's has succeeded in its mission, and the editorial teams over the intervening years deserve a word of praise for this achievement. In this context, it is a privilege and honor to be invited to now serve as an associate technical editor for Electronics Cooling, and help perpetuate Electronics Cooling's mission in serving the electronics cooling community.

To help maintain this momentum, and given that this is my first editorial, I would like to outline my personal views for possible improvements on the dissemination of ongoing knowledge in the electronics cooling community. Having worked on the thermal management of electronic systems in both industry and academia for over two decades, I appreciate where the focus of these two communities ultimately lie in the pursuit of knowledge. Electronics cooling conferences in the past have served a pivotal role in facilitating the exchange of ideas and information between these communities. As my Ph.D. advisor eloquently said to steady my nerves before my first oral presentation at an international conference, "Don't worry if you make a mess of the presentation, it's the publication that has the lasting impression." Is this comment still of value today, given the declining archival quality of many conference publications? To set out this view, I recall that when I was a graduate student in the early 1990s, the peer review process of electronic cooling conferences appeared to be more rigorous and selective than today for the same conferences. Although some authors may receive reviews of a similar standard as in the past today, many others will receive no more than a paragraph in length of comments that may be of limited assistance in improving their paper. Conferences for various reasons appear to now inadvertently focus on "What's New, NOW?" and not necessarily on the "everlasting truth." This raises the question as to what should be the future role of electronics cooling conferences, and where is their value proposition?

In this line of thought, I would like to cite two early Electronics Cooling articles contributed by Moffat [2] and Belady & Minichiello [3] in 1999 and 2003, respectively, that have as much archival value today as at the time of their publication. Moffat outlined the need for uncertainty analysis in the planning stages of an experiment to judge the suitability of the instrumentation; during the data-taking phase to judge whether the scatter on repeated trials is "normal" or means that something has changed; and in reporting the results, to describe the range believed to contain the true value. How many conference papers today incorporate "error bars" in plotted experimental data, or a basic assessment of measurement uncertainty? Belady & Minichiello summarized the necessary framework of a thermal design methodology which comprised three distinct phases: concept development, detailed design, and hardware test.

This methodology suggested at which phase of the thermal design cycle correlations, numerical analysis and experimental prototype characterization should be most applicable. Today, many conference papers present numerical predictions with little or no form of validation, no discussion of solution independence to computational domain or discretization, or no documentation of solution convergence.

Continued on page 32

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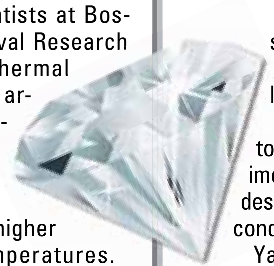
Cooling Matters

Applications of thermal management technologies

THERMALLY CONDUCTIVE MATERIAL COULD REPLACE DIAMOND IN DEVICES

Researchers have identified a material with extraordinarily high thermal conductivity that could replace diamond as an effective thermal management material and lower the manufacturing costs of electronic devices.

New research from scientists at Boston College and the U.S. Naval Research Laboratory has found the thermal conductivity of cubic boron arsenide — a chemical compound of boron and arsenic — is more than than 2,000 Watts per meter per Kelvin at room temperature, and even higher than diamond at higher temperatures.



Boron arsenide was not expected to be a good thermal conductor, but study co-author David Broido said the team used a recently-developed theoretical approach for calculating thermal conductivities, which had tested previously on other well-studied materials. In addition to the development of new passive cooling solutions, the research may also provoke a reevaluation of the guidelines used to predict the thermal conductivity of materials.

Source: Physical Review Letters

NANO-SCALE TRANSISTORS MAY LIFT HEAT DISSIPATION LIMIT IN TINY ELECTRONICS

A quantum-tunneling device created without semiconducting materials by scientists at Michigan Technological University could find use as a nano-scale transistor in tiny future electronic devices.

Physicist Yoke Khin Yap said the size of transistors based on semiconductors is finite, which places a limit on the size of electronic devices. Scientists have previously attempted to address these issues through experimentation with different materials and designs, but have always employed semiconductors like silicon in their research.

Yap and his research team grew "virtual carpets" of boron nitride nanotubes (BNNTs) and placed tiny quantum dots of gold on the tops of the BNNTs to form QDs-BNNTs. Upon applying voltage to electrodes at both ends of the QDs-BNNTs at room temperature, scientists observed electron movement between gold dots, suggesting that the application of sufficient voltage altered the device from its natural state as an insulator to a conducting state. Lowering or turning of the voltage entirely allowed the structure to revert back to an insulating state.

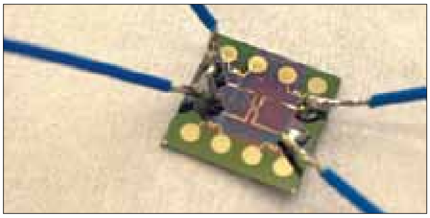
Source: Advanced Materials

GRAPHENE HEAT SPREADER REDUCES ELECTRONICS HOTSPOT TEMPERATURES

Use of a graphene in silicon-based electronics could help increase energy efficiency by significantly reducing hotspot temperatures inside processors, an international team of researchers has claimed.

The new findings are the result of efforts to develop more efficient, portable thermal management solutions. Led by scientists at Chalmers University of Technology in Sweden, the research team found that multiple layers of graphene demonstrate strong heat conducting properties that could be used to remove heat from inside electronic devices. In their study, the researchers focused on altering the temperature in the most heat-intensive areas of an electronic device—such as inside a processor—reducing it by as much as 25 percent. The findings could be a major breakthrough for data center cooling.

Source: Carbon



Datebook

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OCTOBER 28-29

LEDs & the SSL Ecosystem 2013
BOSTON, MASS, US
www.ledsconference.com

OCTOBER 27-29

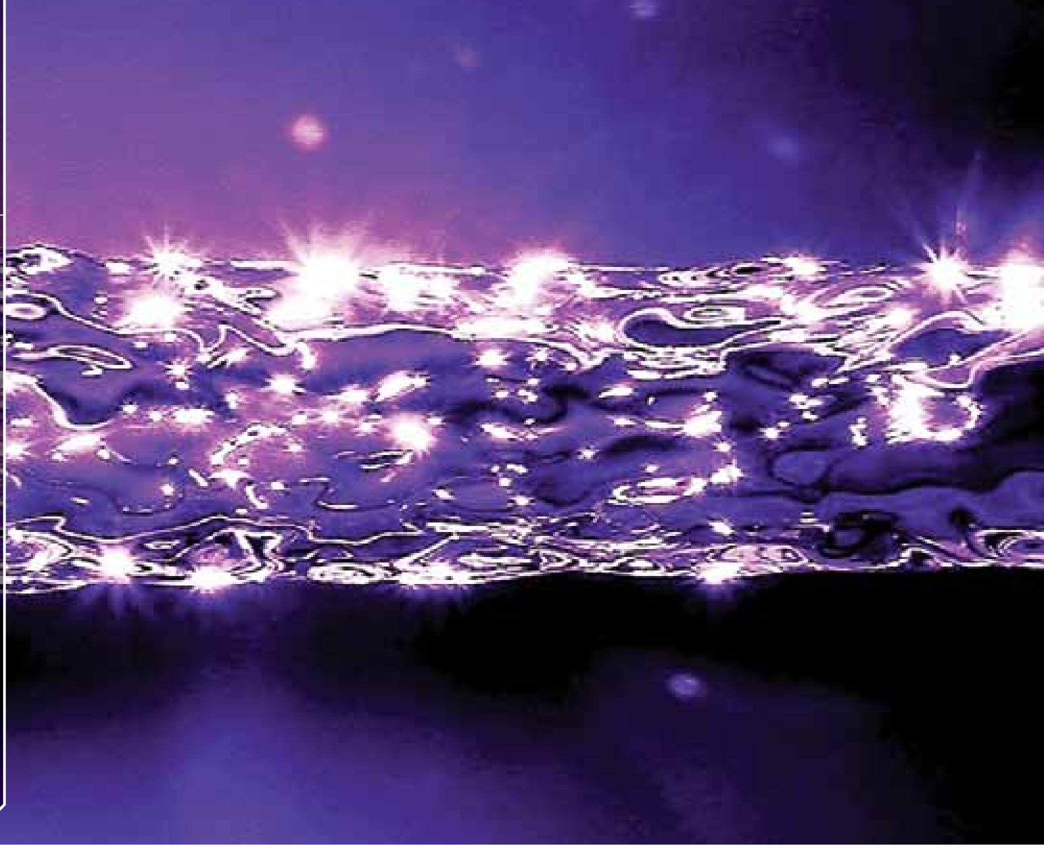
Electronic Components Industry Assoc. 2013 Executive Conference
CHIGAGO, ILL, US
www.eciaonline.org/meetings/ExecutiveConference/2013/index.htm

RESEARCHERS IDENTIFY KEY ATTRIBUTE IN SURFACE DISSIPATION OF HEAT

A team of MIT researchers has completed what they claim is the first systematic investigation of the factors that control boiling heat transfer from a surface to a liquid, a process that is considered crucial to the efficiency of power plants and the cooling of high-power electronics.

The research focused on the relation of material surface attributes to critical heat flux (CHF) limit, a value of heat transfer, per unit time and area, at which the efficiency of a surface's heat-transfer ability is affected. The new findings could reportedly raise the value of CHF and lead to safer nuclear reactors, more efficient heat exchangers and better thermal management of high-power electronics.

Source: Applied Physics Letters



NEW DISCOVERY COULD CHANGE TEXTBOOK MODELS ON HEAT TRANSFER

A discovery in the physics of heat transmission along nanowires could rewrite the models of heat transfer in current textbooks.

Researchers at the National Taiwan University's Center for Condensed Matter reportedly found ballistic thermal conduction by phonons at room temperature along silicon-germanium nanowires.

The successful display of the phenomenon using a common semiconductor and at room temperature could help to realize the development of heat waveguides, terahertz phononic crystals and quantum phononic/thermoelectric devices ready for integration into existing silicon-based electronics.

Source: Nature Nanotechnology

DATA CENTER COOLING SOLUTIONS MARKET IN ASIA TO DOUBLE BY 2018

New market analysis from business consulting firm Frost & Sullivan has suggested the data center cooling solutions market in the Asia-Pacific will double by 2018.

The report, "Asia-Pacific Data Center Cooling Solutions Market," estimates the market-generated revenues of more than $1.2 billion in 2011 will reach $2.17 billion by 2018. Data center operators from other countries, including Apple and Google, are also relocating their data centers to the Asia-Pacific, further contributing to market growth in the area.

Source: Frost & Sullivan

RESEARCHERS TEST EVAPORATIVE COOLING SYSTEM IN ZERO-GRAVITY

University of Illinois at Chicago researchers have completed high- and zero-gravity testing of an evaporative cooling system developed for sophisticated microelectronic systems onboard an astronaut training aircraft following three years of preparation supported by NASA.

Developed to cool the electro-optical and infrared sensors, recording equipment and data processing systems of satellites, rockets and drones in near and outer space, the UIC evaporative cooling system uses thin nanofiber mats to increase cooling efficiency by trapping coolant against the surface so that evaporation is quick and complete.

Source: University of Illinois

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How Useful are Heat Sink Correlations for Design Purposes?

Clemens J.M. Lasance
Guest Editor, Philips Research Emeritus, Consultant@SomelikeitCool

I ASSUME EVERYBODY AGREES with the fact that it is pointless to devote precious space in this magazine to highlight again all problems related to thermal management of electronic products and systems, so let's start right away.

An important way of reducing the temperature in an optimal way is by a proper choice of a heat sink. Apart from the fact that in many applications the design freedom is limited, often due to space or weight requirements, the designer is also confronted with the following problem areas:

- Many new developments, in manufacturing as well as in layout (extruded, corrugated, pin fin, metal foam, narrow channel, enhanced plastic, etc.)
- Many criteria to base an optimal choice on (performance, weight, volume, cost)
- Manufacturer's data are often rather limited in practice because they often are derived for closed ducts
- Data need to include pressure drop
- Standard correlations fail for many practical cases (usually only valid for confined heat sinks)
- Not having a fan does not mean we talk natural convection at the system level
- Detailed CFD modeling at the system level is often not an option unless time, a supercomputer and a calibration lab are available.

FIGURE 1: Pictures of heat sinks used in the LED world (see the web for more examples)

Since literally thousands of heat sinks are available, the designer faces the question: which one? The fact is that too often the choice is based only on cost and vendor data, the problem with the latter being that often their practical usefulness is debatable because they are almost exclusively based on measurements in a closed duct, thereby disregarding bypass effects and inflow conditions. Of course, this applies to forced convection. However, be aware that at the system level we often don't talk natural convection at a local level. This was realized a long time ago, and around the mid-nineties the ASME K16 committee took the initiative to tackle this problem. Belady [1] reported first results. However, as far as I know, no final report has been published, despite the impressive list of highly qualified members of the committee, proving the difficulty of finding a satisfactory solution. I am afraid not much has changed since. The conclusion must still be that vendor data at best can be used for comparison purposes but should be treated with great care when these data are going to be used for final design. So, if vendor data are of limited use, what is the alternative? And here is the fairy tale: use impressive-looking correlations. What's wrong with this? Well, most equations are based on the following assumptions:

- parallel plate heat sinks
- fully ducted flow
- fully developed flow
- strong impact of 3D flow not considered (especially in natural convection)
- equal number of fins and channels
- negligible entrance and exit effects
- laminar and uniform approach flow
- no temperature gradient in heat sink base
- heat spreading effect of base not taken into account
- uniform fin temperature (both between fins and within a fin)

Now have a look at Figure 1 (opposite page) showing a plethora of heat sinks developed for LED applications.

Obviously, if you use handbook equations to base a design upon, chances are high that you miss most of the heat sinks shown above. Indeed, extrusion-based parallel-plate heat sinks are the cheapest around, but they score badly when it comes to optimization of shape/weight/volume/performance, especially regarding optimal fin thickness. What I find remarkable in 2013, is that purchasing departments still play a major role in deciding what kind of heat sinks are to be preferred, often based upon cost (and aesthetical) arguments only. Not much changed since the seventies, the days when Philips Elcoma manufactured 4 billion resistors a year, and when Philips TV sales people tried to find a vendor operating from a shed somewhere in Asia who would sell a couple of hundred resistors that would go into a single TV for 0.01 cent a piece less. The price of a TV in those days was 2000 dollars. The same kind of sub-optimization is still going on in the LED world. Nothing new of course, look what the banks are doing nowadays, after having caused a lot of misery worldwide only a few years ago. You can't teach an old dog new tricks.

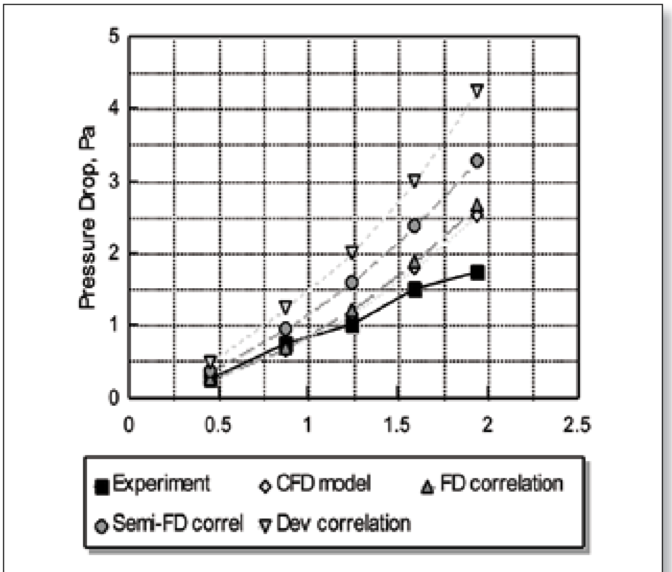

FIGURE 3: Pressure drop results for typical heat sink. X-axis parameter: velocity in m/s, FD: fully developed flow, Dev: developing flow

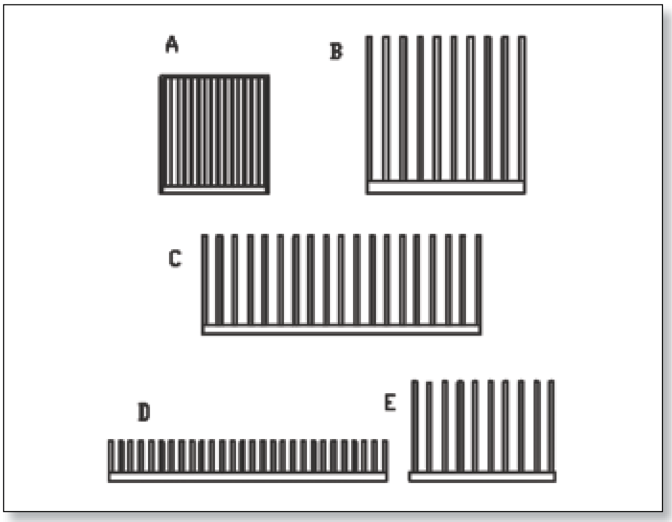

FIGURE 2: Heat sinks tested by Biber and Belady [2]

For designers that are not convinced or prefer black parallel-plate heat sinks (de gustibus et coloribus non est disputandum), here is something to reconsider. A long time ago Biber and Belady [2] realized that the pressure drop is one of the most important parameters because it determines the velocity and consequently the heat transfer. They compared correlations for developing and fully-developed flow with test and CFD results for a number of heat sinks, see Figure 2.

For purpose of illustration, the pressure drop results for a typical heat sink (not specified here) are shown in Figure 3.

As you may notice, we are not talking peanuts here. Even for rather low velocities around 1 m/s the differences are of the order of 50-100%, at least for the correlations. CFD results start to differ above 1.5 m/s, which could be due to the flow model and meshing used. Maybe high time that somebody repeats this analysis using state-of-the-art CFD? The authors concluded that not only the correlations were of limited use when it comes to accuracy but also that the prevailing test methods should be improved since no standardized test method did exist. Note for the experienced reader: be aware that this is a column, not an article. This example is just to illustrate that the matter is much more difficult than is suggested by the correlation worshippers.

CONCLUSION

Designers of the world: unite! Convince your bosses that it pays off to optimize at the system level, not at the part level. And in such a world there is no place for correlations that are exclusively based on single parallel-plate heat sinks in wind tunnel flow, unless of course your application requires such a fin and is used in a wind tunnel.

Are there alternatives? Sure, recommended approaches are:

- Dedicated tests to rank a series of heat sinks
- CFD with calibrated heat sink compact models
- Prototype testing in a realistic enviroment

These approaches are discussed in [3].

Finally, I highly recommend to repeat the CFD analysis and experiments as published by Biber and Belady [2], using state-of-the-art CFD codes. Additionally, as proposed by me on a JEDEC meeting in March 2012, we need a revival of the Working Party that started in 1995 to address proper standardization practices. Last but not least, there are still too many US vendors that use only US units, as if the US is the only country that matters.

FURTHER READING

Introductory texts using design equations for forced convection heat transfer can be found in Biber [4, 5, 6], and in an overview of Calculation Corner topics that appeared in the ElectronicsCooling Magazine over the past ten years or so [7]. Also recommended is the famous book by Kraus and Bar-Cohen [8]. More on the few pros and many cons of correlations, see Lasance [9].

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Thin Film Thermal Conductivity Measurement using a Micropipette Thermocouple

R. Shrestha, K. M. Lee and T. Y. Choi, University of North Texas
D. S. Kim, POSTECH

INTRODUCTION

DUE TO THE REQUIRED experimental characterization complexity for the thermal conductivity measurement of thin films, accurate measurement of such materials has been difficult to achieve for thicknesses less than 1 μm. For example, conventional Fourier heater plate methods have proven inapplicable as the thermal resistance between the film and the plate is the dominating measured quantity, rather than the thermal resistance of the thin film itself [1]. Furthermore, when large temperature sensors (smallest ~50 μm) are used, the conductive heat loss through the sensors may be larger than the heat flow through the thin film, making it difficult to measure the film thermal conductivity. In an effort to resolve these issues, laser source heating, rather than a heating strip, was employed in combination with a high sensitivity, high resolution glass-based micropipette thermal sensor. This laser heating and micro scale sensor combination allows for accurate measurement of ±0.01°C of temperature differences while minimizing heat loss through the sensing tip and eliminating thermal resistance issues between heating strips and thin film interfaces. Such thermal response measurements have previously been demonstrated using pipette based sensor technology [2-4]; however, these micropipette sensors have had limitations regarding measurement accuracy and reliability (e.g., deterioration of the sensor tip resulting from repeated use). The complex fabrication process, cost effectiveness and small thermo power of the sensors were also potential limitations.

FABRICATION OF THE SENSOR

In order to overcome such limitations, a novel glass micropipette sensor was developed to permit accurate measurement of thin film thermal conductivity. A pipette puller (P-97, Sutter Instruments) was programmed according to a known recipe for creating patch pipettes with a tip size of approximately 1 μm and 5 to 7 mm taper length. It was used to pull a thick-wall borosilicate glass tube, with 1.5 mm outer diameter and 0.86 mm

Kyung-Min Lee is currently senior research scientist at Terra Instrument. He was working in Mechanical and Energy Engineering department at the University of North Texas as post-doctoral research associate. He received his Ph. D in Physics at UNT. His major research area is nanoscale materials applications and characterization such as thermal properties of nanowire and nanotube, optoelectrical characterization of semiconducting nanostructures (Si, SiC, ZnO, CNT, and graphene), and biological applications including development of cellular level temperature detection system and of imaging device.

Ramesh Shrestha obtained his master's degree from Mechanical and Energy Engineering, University of North Texas in 2011. He is currently a Ph. D. student under the supervision of Prof. Tae Youl Choi. He has published journal articles in Sensors and Rev of Sci Instrum. His publications reflect his current research interests in development of high precision micropipette thermal sensors for the thermal characterization of carbon nano tubes and graphene thin films and real time thermal characterization of biological cells.

Tae-Youl Choi is an Associate Professor of Mechanical and Energy Engineering Department at the University of North Texas. He has earned his BS and MS from Seoul National University. And he is awarded PhD from University of California, Berkeley in 2002. He was a lecturer at the Department of Mechanical and Process Engineering at ETH Zurich, Switzerland before he joined UNT in 2006. His major expertise in research is micro/nanoscale thermal and fluid science and engineering.

Professor Dong Sik Kim received his Ph. D. degree from UC Berkeley (USA) in 1998. After serving as an Assistant Professor in the Mechanical Eng. Department at UT Austin (USA) for two years, he joined POSTECH (Korea) in 2000 and is currently a Professor in the Mechanical Eng. Department. His research interests are in laser materials processing and microscale energy transport, with emphasis on laser interaction with materials at micro/nanoscales and microscale thermal analysis/sensors.

inner diameter, into a micropipette. Similar pipettes are often used in various biological applications for injecting solutions into biological tissue. The pulled pipette was filled with a lead-free soldering alloy composed of mostly tin (Sn) through an injection molding process in conjunction with localized heating of the material. The injection molding was accomplished by mechanical pressurization (or pushing) of molten metal at the upper part of the pipette while simultaneously heating the lower part near the pipette tip with an electronic soldering gun maintained at around 250 °C.

Followed by the molding process, the pipette tip was beveled in order to remove any unwanted extruding metal. This step is particularly important to assure a smooth and continuous contact between the two metals in the formation of a thermocouple. Therefore, the BV-10 micropipette beveller (Sutter Instruments) which was designed for beveling micropipettes with tip diameters between 0.1 and 50 μm was used to sharpen and smoothen the pipette tip. After beveling, the pipette was cleaned with ethyl alcohol using an ultrasonic cleaner. Following the cleaning process, a sputtering technique was used to coat thin films of nickel on the outer surface of the glass and thus form a Ni-Sn alloy junction at the beveled tip. This process was successfully used to develop a thermal sensor with micrometer sized sensor tip (Figure 1). The size of the sensor in the study is only a few microns. Thus, the sensor can detect temperature distribution of a few micron sized area. Spatial resolution of the sensor is determined by the size of the sensor. Because of micron-scale size, the lost power transmitted through the sensor tip turns out to be negligible as compared to the absorbed laser power. This fact was confirmed by accurate measurement of thermal conductivity of a stainless steel thin stripe (not published).

Figure 1e depicts the two lead wires that separately connect the Ni coating and the Sn-alloy core of the pipette to a terminal on an isothermal aluminum block. The lead wires have the same composition of the material they connect to. At their respective terminals on the block, each lead wire is joined to a copper extension wire. Together, the contact regions between the lead wires and the copper wires form the cold junction for the measurement. This was done so that any unwanted thermocouple effects from the cold junction could be removed. The copper wires provide the connection to the nano-voltmeter.

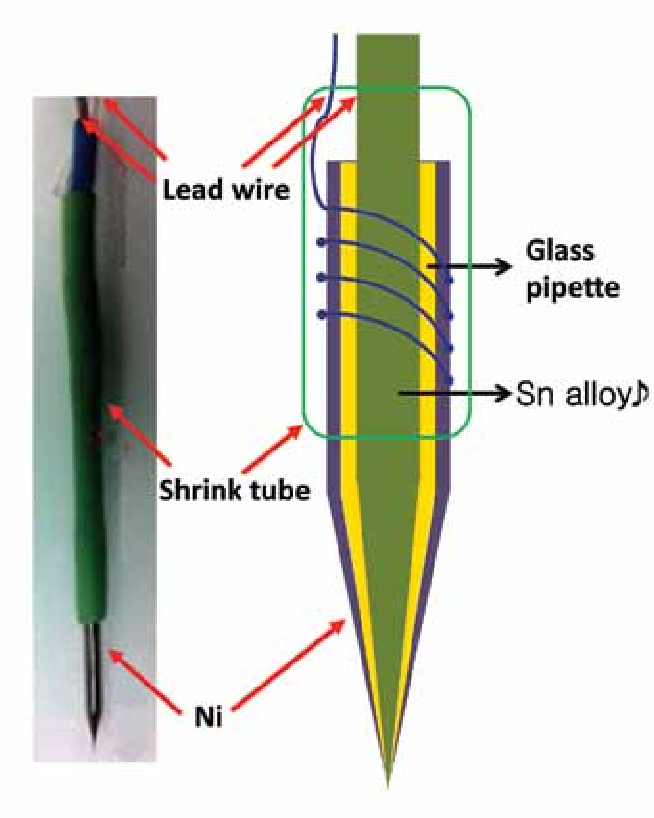

FIGURE 1: A completed micropipette thermal sensor with its schematic outline.

CALIBRATION OF THE SENSOR

Calibration of the fabricated sensor was conducted with a water-filled chamber maintained at constant temperature with an accuracy of ±0.01°C. A high-precision digital thermometer and the fabricated sensor were immersed into the water bath to read out an actual temperature of the wateDuring the calibration process, the cold junction was maintained at a constant temperature (e.g. 24.5°C) slightly above room temperature." The voltage generated by the sensor was recorded by a voltmeter (Nano Voltmeter, Keithley 2182) and compared to the temperature read by the thermometer. In this way, variation of voltage with temperature difference ($\Delta V/\Delta T$) was obtained for the thermoelectric power, i.e. Seebeck coefficient. The standard deviation in the voltage measurement was less than 0.018 μV which is equivalent to temperature rise of 0.002°C, which is one order of magnitude lower than the temperature measurement accuracy of 0.01°C.

APPLICATION OF THE SENSOR

As an application for the sensor, thermal conductivity measurements of a single walled carbon nanotube (SWNT) film suspended over a hole in a poly-carbonate substrate were made. The CNT film consisted of SWNTs randomly oriented in the plane of the film, without any matrix material (such as a polymer) being present. To produce a film of SWNT, a vacuum filtration method was employed which involves vacuum filtering a dilute suspension of nanotubes in a solvent over a porous alumina filtration membrane (Whatman, 200 nm pore size, 47 mm diameter). A schematic of the measurement setup is shown in Figure 2. Antireflection coated lenses were used to collimate and expand a ray of beam which was then diverted at 90° by a beam splitter toward the CNT film. A 20× super-long working distance objective lens (Mitutoyo MPlan Apo SL) converted the diverted beam to a Gaussian beam profile of 3 μm spot size on the CNT film. A class B laser at 532 nm was irradiated at the center of the suspended, 50-μm CNT film (thickness of 100 nm). The charged-coupled device (CCD) camera as shown in Figure 2 was used to obtain clear images of laser spot and the sensor tip. The inset in Figure 2 shows CCD images of (a) laser shined at the center of the film and (b) the pipette sensor positioned on the film.

The temperature difference at two radial positions was measured using the pipette sensor with tip size approximately 3.5 μm, and Seebeck coefficients of 5.67 μV/°C. The same procedure was repeated using a different pipette sensor with the same tip size and Seebeck coefficient of 7.44 μV/°C, to enhance the measurement reproducibility. The voltages at the two different locations, approximately 8 μm apart in radial directions, were measured with known Seebeck coefficients, and then converted to temperature difference. The power absorbed by the CNT film was determined to be approximately 75% of the total irradiated power. The absorbed power was calculated according to the relationship $P_{absorbed} = P_{incident} - P_{reflected} - P_{transmitted}$. The thermal conductivity was determined to be 73.4 W/m°C using

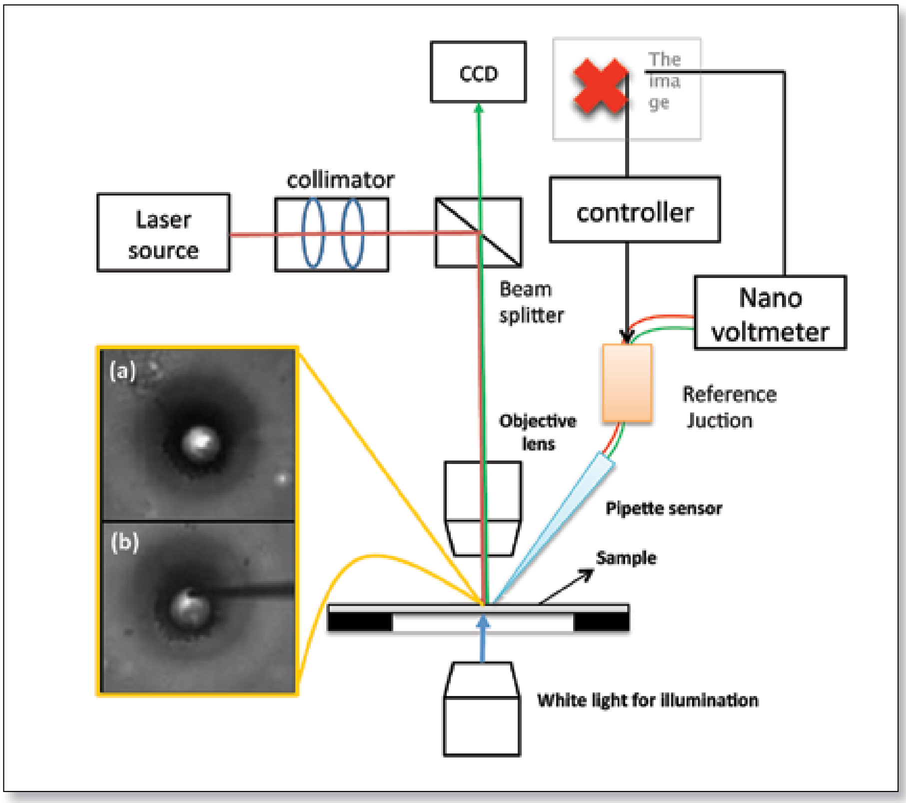

FIGURE 2: Experimental setup for the thermal conductivity measurement of CNT film with the micro-pipette sensor. The inset: CCD image of (a) laser shined at the center of the film and (b) the pipette sensor positioned on the film.

equation 1, which is derived for one dimensional radial heat conduction in a cylinder.

$$\text{(1)}\quad \dot{Q} = \frac{2\pi k t (T_1 - T_2)}{\ln\left(\frac{r_2}{r_1}\right)}$$

where $\dot{Q}$ is the power absorbed, k is the thermal conductivity of CNT film, t is the thickness of CNT film, r_1 and r_2 are radii of two locations, and T_1 and T_2 are the temperatures at two radial positions.

Measurement of thermal conductivity of SWNT film has been rarely made elsewhere except for this study. However, measurements of thermal conductivity of multi-walled carbon nanotube (MWNT) films were made by other groups which showed varying values from 1.52 W/m°C to 83.0 W/m°C [5-8]. In addition, we have performed a thermal conductivity measurement at room temperature for a thin (~1 µm thick) stainless steel stripe using micropipette thermal sensors (not published). Repeated measurement results for stainless steel stripes revealed good agreement with literature value.

CONCLUDING REMARK

The developed technology can be applicable to electronic devices and integrated micro/nano-electro-mechanical systems (MEMS and NEMS) due to the feasibility in measuring temperature at a highly localized hot spots with high spatial (few micron), and temperature resolutions (<0.01°C). Moreover, usefulness of the micro thermocouple sensor is extended to biological purposes; intramembranous cell temperature measurements have previously been made by our group to assess cell temperature rise due to laser irradiation [9].

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Calculating the Heat Dissipation Rate for a Vapor Condenser Heat Sink

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THIS ARTICLE PRESENTS AN analysis methodology that can be used to calculate the thermal resistance of a vertical downward facing vapor condenser plate-fin heat sink, i.e. a heat sink in which the plate-fins extend downward from a horizontal base into a coolant vapor region and whose function it is to condense this vapor into liquid condensate. Such heat sinks are used in cooling systems where the heat rejection from the source is carried out via a coolant boiling process and this heat is then rejected to an ambient fluid (air or liquid) using a vapor condensation process.

Figure 1 displays an elevation view of a dielectric coolant immersion cooled electronics module in which pool boiling from a "boiling" heat sink attached to the back side of a microprocessor chip is the primary heat dissipation mechanism from the device. The coolant has a boiling point that is much lower than the target surface temperature of the electronic device. For example, the coolant could be HFE7000 [1] which boils at approximately 35°C at atmospheric pressure. If the target boiling fin surface is 60°C, then, this allows for as much as 25°C of superheat (temperature excess) between the fin and the local liquid coolant. The magnitude of boiling heat transfer coefficient on the fin surface, and thus the thermal performance of the heat sink, is dependent on this superheat. A methodology on how to calculate the thermal resistance of such a boiling heat sink was provided by Simons [2]. Applications for pool boiling based cooling of IT equipment have been discussed further in Tuma [3].

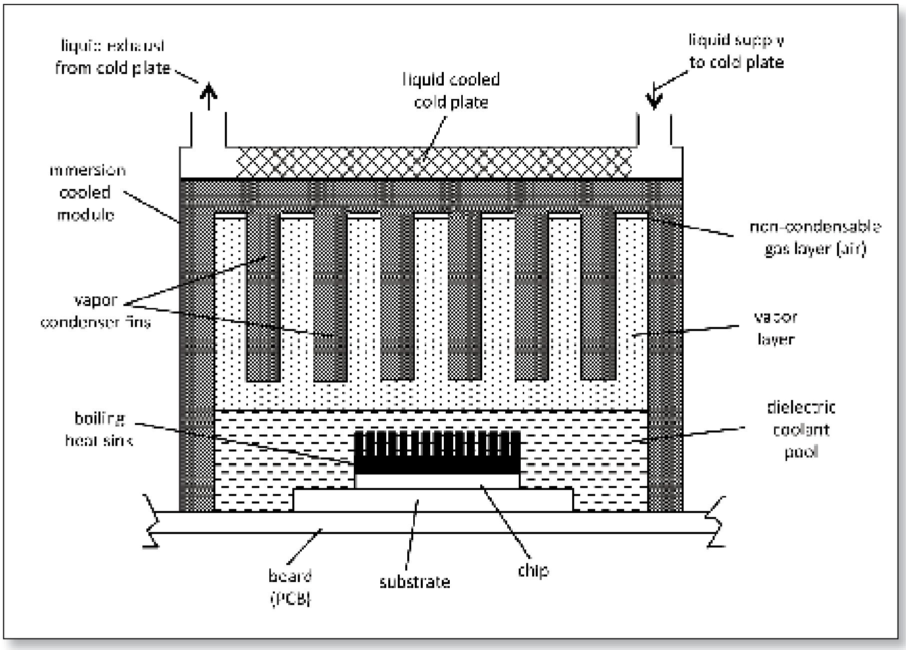

FIGURE 1: Schematic of an immersion cooled module with a vapor condenser

The vapor generated from the pool boiling phenomenon rises to the top of the immersion cooled module where it comes in contact with the fins of a condenser heat sink. The condenser heat sink is attached via a thermal interface material to a liquid cooled cold plate with liquid flow at a temperature lower than the boiling point of the encapsulated vapor. The cold plate serves to transfer the module heat load from the immersion coolant to the liquid loop circulating at the system level. The vapor in contact with cool condenser fins condenses into a liquid film which flows downwards along the length of the fin. Thus, as depicted in Figure 2(a), the condensate film grows thicker along the length of the vertical surface (i.e. the fin), in the downward direction against gravity, and at the end of the fin, the condensate droplets that form, fall back into the liquid pool that submerges the electronics chip. Also depicted in Figure 1 is a non-condensable gas layer, which is usually air that was dissolved in the coolant. The impact of this thin layer on the thermal performance of the heat sink will be ignored in this analysis.

Figure 2(b) shows the variation of

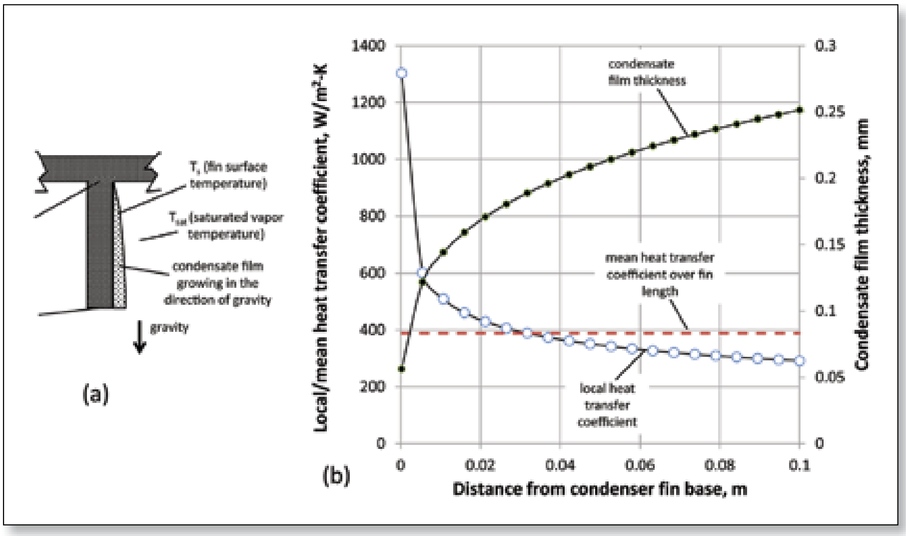

FIGURE 2: Liquid film on a vertical condenser surface, **(a)** Schematic of phenomenon, **(b)** Variation of the heat transfer coefficient with distance from fin base as predicted using equations (1)-(4) and Table 1 parameters.

the local condensation heat transfer coefficient at increasing distance from the base of the condenser fin for the conditions described in Table 1. Several of the thermodynamic values were calculated using commercial software [4] or from coolant literature [1]. The values for the local and mean heat transfer coefficient and the local condensate film thickness are calculated using the Nusselt equations for laminar flow of condensate over a vertical flat plate that has been provided by Rohsenow [5], and given by,

$$\textbf{1)}\quad h_m = \frac{k_l}{L} Nu_L = \frac{k_l}{L}\, 0.943 \left\{ \frac{\rho_l(\rho_l-\rho_g)\, g\, h_{fg}^{*} L^3}{\mu_l k_l (T_{sat}-T_s)} \right\}^{1/4}$$

$$\textbf{2)}\quad h_l = \left\{ \frac{\rho_l(\rho_l-\rho_g)\, g\, h_{fg}^{*} k_l^3}{4\,\mu_l (T_{sat}-T_s)\, z} \right\}^{1/4}$$

$$\textbf{3)}\quad \delta_l = \left\{ \frac{4\,\mu_l (T_{sat}-T_s)\, z\, k_l}{\rho_l(\rho_l-\rho_g)\, g\, h_{fg}^{*}} \right\}^{1/4}$$

where, Nu_L is the Nusselt number averaged over the length L, z (m) is the distance from the fin base in the downward vertical direction, g is gravitational acceleration (9.8 m/s^2), and h_{fg}^* is a effective latent heat of evaporation that is given by,

$$\textbf{4)}\quad h_{fg}^{*} = h_{fg} \left\{ \frac{1+0.68\, C_p (T_{sat}-T_s)}{h_{fg}} \right\}$$

Observing Figure 2(b), one can see that as the condensate film gets thicker the local heat transfer coefficient drops significantly, because the heat has to be conducted through the liquid film thickness. It should be noted that the equations (1)-(4) are for laminar condensate flow. After a certain fin height though, the flow could turn to laminar wavy or turbulent yielding higher heat transfer coefficients. This aspect is beyond the scope of this article. Interestingly, the absolute values for the film thickness are quite small even for long fins (e.g. 0.1 m) as shown in Figure 2(b). So, it would not be difficult to design a heat sink that has a wide enough gap between the fins to accommodate the film thickness growth.

The analysis in Figure 2(b) does not take into account any temperature drop along the length of the fin, i.e. it does not capture fin efficiency, which one would expect, would be an important factor given that the heat transfer coefficients are so high (Figure 2(b)) and that the temperature difference between the surface and the vapor is itself an parameter used to calculate the heat transfer coefficient (equation (1)). Thus, accounting for the fin efficiency effect in equation (1), we get,

$$\textbf{5)}\quad h_{m,fin} = \frac{k_l}{L}\, 0.943 \left\{ \frac{\rho_l(\rho_l-\rho_g)\, g\, h_{fg}^{*} L^3}{\mu_l k_l (T_{sat}-T_s)\, \eta_{fin}} \right\}^{1/4}$$

where η_{fin} is the fin efficiency, which can be calculated using,

$$\textbf{6)}\quad \eta_{fin} = \tanh(mL)/mL$$

where m is a fin parameter and given by,

$$\textbf{7)}\quad m = [h_m P/kA]^{0.5}$$

where P, is the fin perimeter, k is the fin material thermal conductivity, and A is cross-sectional area of the fin. For a fin whose width is D and thickness is t, the perimeter P is equal to 2(D+t) and the cross-sectional area is equal to Dt. For a very thin fin, the P can be approximated to 2D which allows the m to be approximated to $[2h_{m,fin}/kt]^{0.5}$. It should be noted that equation (7) is based on several assumptions including an insulated fin tip, a constant heat transfer coefficient, and quassi 1-D heat flow through the fin.

Using the mean fin heat transfer calculated using equation (5), the condensation heat sink heat dissipation rate can be calculated using,

$$\textbf{8)}\quad Q_{fins} = N\, \eta_{fin}\, h_{m,fin}\, A\, (T_{sat} - T_{base})$$

where N is the number of fins. N can be approximated to be W/(s+t), where W is the width of the heat sink, s is the fin to fin gap, t is the fin thickness, and the number of fins and gaps are equal or there are a large number of fins. If there are N fins and (N-1) gaps, i.e. both ends of the heat sink has fins, then W = Nt + (N-1)s. If there are N fins and (N+1) gaps, i.e. both ends of the heat sink has gaps, then W = Nt + (N+1)s.

In equation (8), A is the surface area of the fin that is given by,

9) $A = 2L\,(D+t)$

Equations (8) and (9) ignore the contribution of the exposed base area of the heat sink that is in contact with the coolant vapor. This is valid for long fins where the fin area is much larger than the exposed base area.

The thermal resistance of the condenser fins can then be calculated using,

10) $R_{fins} = 1 / N\,\eta_{fin}\,h_{m,fin}\,A$

The total thermal resistance of the condenser is thus the sum of the base and fins thermal resistance, and given by,

11) $R_{condenser} = R_{fins} + t_{base}/(k_{base}WD)$

where t_{base} is the thickness of the condenser base.

Thus, the total heat dissipation rate of the condenser heat sink can be calculated using,

12) $$Q_{condenser} = \frac{[T_{sat} - T_{base}]}{R_{condenser}}$$

where T_{base} is the base temperature of the condenser that interfaces with the liquid cooled cold plate.

Figure 3 shows predictions for calculating the heat dissipation from a vapor condenser of different sizes and made from three materials using equations (5)-(12). The geometry and material assumptions utilized for the calculations are provided in Table 2.

As may be seen from Figure 3, the vapor condenser heat sink cooling capability increases sharply with fin length for short fins, but plateaus after the fins are approximately 0.05m long. For really short fins, e.g. 0.005 m, the fin efficiency is significantly high (> 0.95), and there is minimal difference between different materials such as magnesium, aluminum, and copper which have thermal conductivities in the 150-400 W/m-K range. For the calculations presented herein, the assumption that the fin base temperature is approximately equal to the base of the condenser heat sink has been made. This is valid for a thin condenser base. It should also be highlighted than the fin efficiency equation cited in equations (6)-(7) is applicable only for long thin fins. Consequently, while results are presented herein for short fins (5-30mm), the author cautions the user if they use data for short fin lengths (e.g. < 30 mm), as the temperature distribution in the fin might be significantly 2-D and thus the fin efficiency equation used may not

TABLE 1: INPUT PARAMETERS FOR CALCULATIONS SHOWN IN FIGURE 2(B)

Parameter	Symbol	Units	Value
Length of vertical surface (fin)	L	m	0.1
Temperature of vertical surface (fin)	T_s	°C	25
Coolant type	--	--	HFE7000 [1]
Temperature of saturated vapor	T_{sat}	°C	35.3
Liquid density of coolant*	ρ_l	kg/m^3	1399.4
Vapor density of coolant**	ρ_l	kg/m^3	8.34
Coolant liquid specific heat*	C_p	J/kg-K	1076
Latent heat of vaporization	h_l	J/kg	142000
Coolant liquid dynamic viscosity*	μ_l	kg/m-s	0.00039961
Coolant liquid thermal conductivity*	k_l	W/m-k	0.073

NOTE: Coolant properties evaluated at mean condensate film (*) or saturated coolant (**) temperature.

TABLE 2: PARAMETERS FOR CONDENSER HEAT SINK ANALYSES DISPLAYED IN FIGURE 3

Parameter	Symbol	Units	Value
Length of vertical fin	L	m	0.005-0.1
Depth of the fin (along the fin)	D	m	0.1
Width of the condenser heat sink	W	m	0.1
Thickness of heat sink base	T_{base}	m	0.0025
Fin thickness	t	m	0.005
Fin gap	s	m	0.0056
Number of fins	N		10
Fin thermal conductivity	k	W/m-k	156, 200, 400
Saturated vapor temperature	T_{sat}	kg/m-s	35.3
Heat sink base temperature	T_{base}	°C	25.3

be applicable. Also, it should be further noted that the fin spacing assumed must be greater than twice the condensate film thickness for the analyses presented herein to be valid, i.e. the film heat transfer coefficient is considered to be independent of fin spacing. For example, Figure 2(b) shows a maximum condensate film thickness of 0.25mm; thus the fin spacing must be greater than 0.5 mm when applying these equations for the conditions listed in Table 1. The calculation performed using equations (5)-(12) required the solutions of several simultaneous equations with several unknown variables using a commercial software [4].

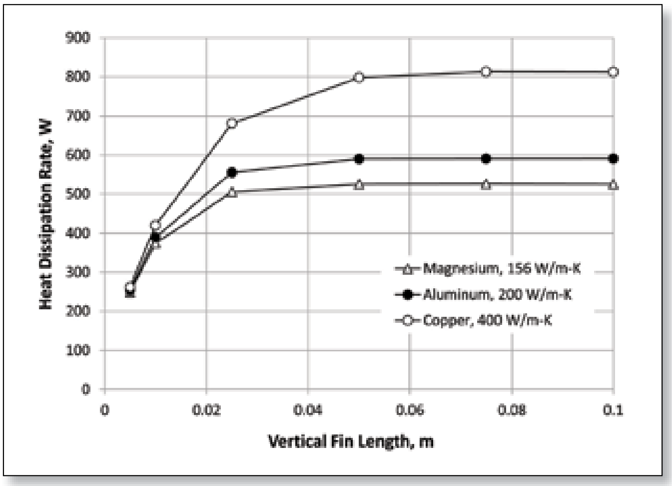

FIGURE 3: Variation of heat dissipation rate with fin length for a vapor condenser heat sink

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Heat Pipe Integration Strategies for LED Applications

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IN LIGHT EMITTING DIODES (LEDS) 70% to 80% of the applied electrical power is converted to waste heat. If this thermal energy is not properly dissipated, the resulting high operating temperatures lead to reduced brightness, shift in wavelength (color), and reduced life. Optical requirements impose the heat to be extracted through circuit boards designed to balance contradictory thermal management and electrical isolation functions [1-5]. In most general lighting applications, the heat must be ultimately be dissipated through natural convection heat sinks (where radiation may play a significant role) due to acoustic noise restrictions [6-14]. However, the thermal management requirements of emerging high intensity LED lighting products often exceed the practical limits of these passive cooling strategies. In the broader electronics cooling industry, heat pipes have been effectively applied as a means to extend the application window of passively cooled heat sinks through heat spreading enhancement. Although the general guidelines for integrating heat pipes in broader electronics cooling applications still apply to LEDs, their unique thermal requirements require adaptation in the implementation of heat pipes. This article explores the implementation and benefits of heat pipes in natural convection heat sinks and circuit boards for LED applications.

Although each LED may only dissipate a few watts of thermal energy, the small package footprint results in high heat fluxes. Despite heat spreading in the LED packages and circuit boards, these heat fluxes remain significant as the heat is dissipated across the various thermal interfaces between the LED package, circuit boards, and attached heat sinks [15-19]. By embedding heat pipes directly into circuit boards, the thermal interface between the circuit board and heat sinks can be minimized while heat spreading can be enhanced. At the heat sink level, heat pipes may be able to reduce the volume for natural convection heat sinks by 10% to 30%. Further, the luminaire design may dic-

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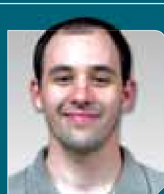

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tate a remote heat sink due to other design considerations, such as aesthetics. In these cases heat pipes enable thermal connection of the remote heat sink to the LED circuit board package with minimal thermal gradient.

1. NATURAL CONVECTION HEAT SINKS

Heat pipes can be effectively embedded in a variety of heat sink form factors to improve conductive heat spreading. To clearly illustrate the benefits of using heat pipes, a radial heat sink with a heat pipe embedded in the core is chosen as a model case as illustrated in Figure 1. In general, heat pipes tend to have increased benefits as the length (*z*) of the heat pipe is increased. This is attributed to the low thermal resistance of the heat pipe's vapor core, which is often negated when compared to other thermal resistances in the system. As a result, the heat pipe's thermal resistance does not change significantly as the heat sink length is increased. To demonstrate this point, thermal finite element analysis was performed on a typical aluminum extrusion radial heat sink with and without embedded heat pipes (see dimensions in Figures 1 and 2). Heat was applied in a $1cm^2$ circular region on one side of the base of the heat sink. In a series of simulations, the length of the heat sink was increased while prescribing a heat transfer coefficient associated with natural convection (10 W/m^2K). Radiation was not considered in the calculations. The simulation results are summarized in Figure 2 which shows the net reduction in thermal resistance (including the heat sink conduction and convection resistance) between the embedded heat pipe and baseline aluminum case. The improvement with heat pipes approaches 30% for heat sinks less than 30 cm long.

The results of Figure 2 are indicative of the performance improvement when the circuit board is directly connected to the base of the heat sink. Heat pipes show more dramatic improvement when the heat sink is remotely located from the circuit board. Figure 3 shows an infrared (IR) image of two heat pipe heat sinks operating in natural convection conditions with 30 Watts of applied heat. A FLIR A655sc camera with +/-2°C accuracy, 640 x 480 resolution, and a spectral range of 7.5µm to 14µm was used. All surfaces on the heat sink were coated with Medtherm optical black coating (specified to a 0.95 average absorptance over a 0.3 µm to 15µm spectral range). The photograph on the left shows the thermal gradient in a 30 cm long heat sink (the other dimensions are identical to those simulated in Figure 2). The increased thermal gradient near the base of the heat sink is noticeably higher than the opposite side of the heat sink. This is attributed to the evaporator thermal resistance of the heat pipe that must be overcome before heat is transferred into the highly conductive vapor core. After the heat is acquired in the first 10 cm of the heat sink's length, the heat sink is nearly isothermal due to the low thermal resistance of the heat pipe vapor space. On the right, the same heat sink is remotely attached to the heat source. The heat pipe clearly demonstrates the transport of heat isothermally from the heat source to the heat sink and apply even distribution of heat to the heat sink. A slight increase in temperature is measured across the heat sink (< 0.5°C), due to the sensible heating of air rising through the heat sink.

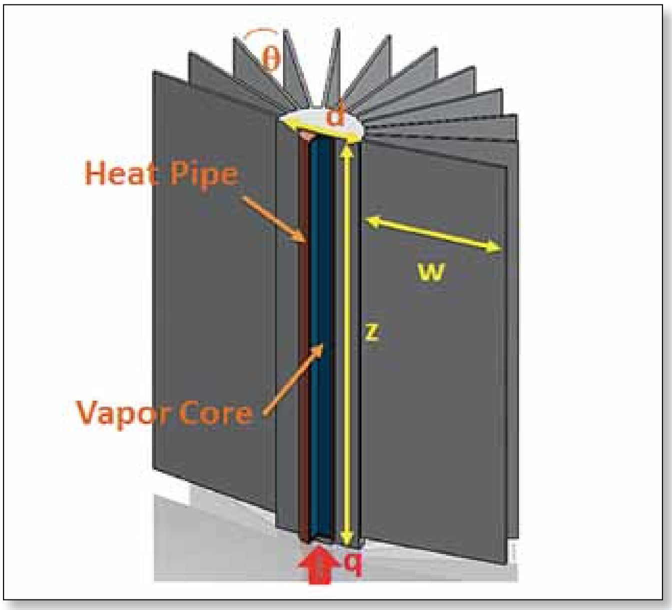

FIGURE 1: Cross-sectional view of a heat pipe embedded radial heat sink.

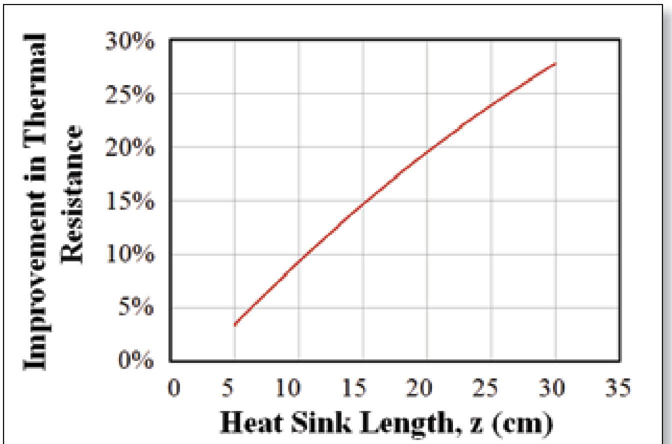

FIGURE 2: Net percent reduction in thermal resistance (including the heat sink conduction and convection resistances) between the embedded heat pipe and baseline aluminum case as a function of heat sink length and heat transfer coefficient. Note: At each point on this chart, a finite element analysis simulation was performed on identical form factor aluminum and heat pipe embedded aluminum heat sinks (8mm embedded heat pipe, θ=18° (20 fins), 1.27 mm thick fins, w=22.2mm, and d=19.1mm) at various heat sink lengths and prescribed heat transfer coefficients.

2. METAL CORE PRINTED CIRCUIT BOARDS

Heat pipes can also be applied at the circuit board level to

improve heat spreading performance [20]. There are several strategies for improvement. One strategy is to fully contain the heat pipes within the printed circuit board, as shown in Figure 4. If the ratio of the heat source to circuit board areas is sufficient, this can be an effective way to improve heat spreading at the board level while requiring minimal design changes to the lighting system. Figure 5 shows an IR image of a fully integrated LED/circuit board/heat pipe assembly during operation.

Another closely related implementation strategy is to simply extend the heat pipe from the circuit board and directly attach the heat pipes to a heat sink. By directly connecting the circuit board to a heat sink using heat pipes, the thermal interface between the circuit board and heat sink is avoided. The improvement in thermal performance is very application specific, and depends on many of the factors described in the natural convection heat sink discussion.

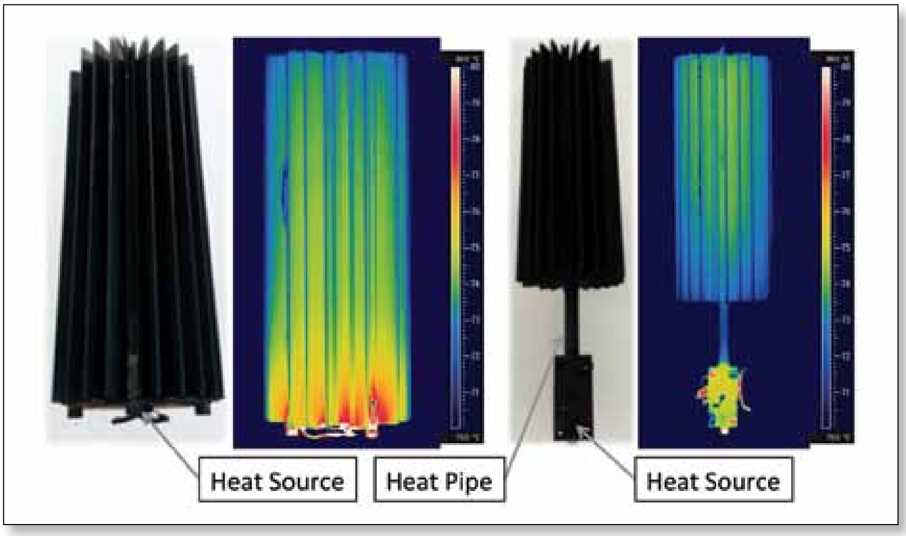

FIGURE 3: IR images and photographs of heat pipe embedded radial heat sinks with direct (left) and remote (right) attachment of the heat source (both scales are set between 70°C and 80°C).

3. CONCLUSIONS

LED lighting products have unique performance and thermal management challenges that must be addressed when implementing heat pipes. Heat pipes can silently and passively improve thermal performance, limit heat sink size, and increase reliability in LED applications. In natural convection radial heat sinks less than 30 cm in length, reductions in thermal resistance approaching 30% can be obtained by simply embedding heat pipes into the heat sink core. Heat pipes can also increase packaging flexibility by enabling remote heat sink location. Finally, overall thermal performance can be improved by directly attaching heat pipes to a circuit board. The performance increase is due to more effective heat spreading and reduction of thermal interfaces.

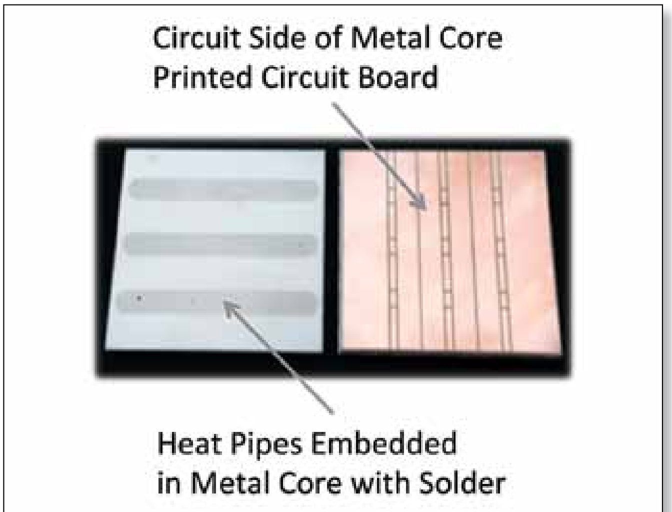

FIGURE 4: Photograph of metal core printed circuit board with heat pipes soldered into the metal core of the circuit board.

4. ACKNOWLEDGEMENT

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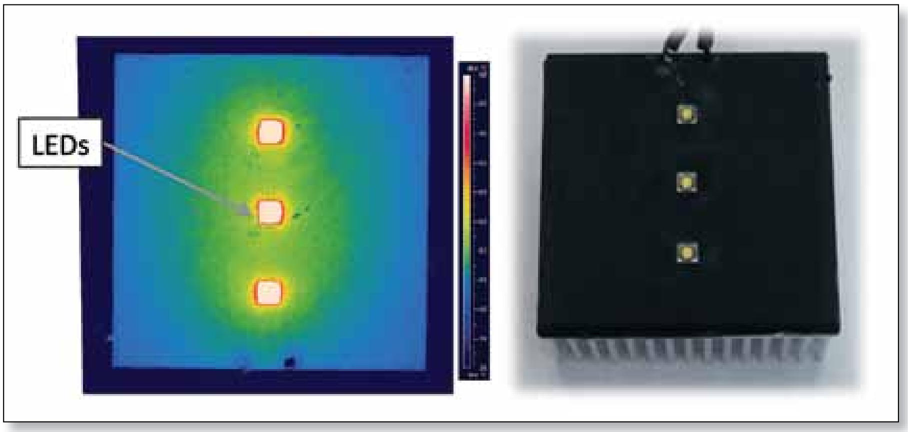

FIGURE 5: IR images and photographs of a circuit board with embedded heat pipes embedded circuit board during LED operation. The temperature scale (i.e., 58°C to 68°C) has been set to emphasize the thermal heat spreading in the circuit board. All surfaces other than the LED packages were coated with Medtherm Optical Black Coating (emissivity =0.95).

Testing of Power LEDs:
The Latest Thermal Testing Standards from JEDEC

András Poppe, PhD
Mentor Graphics MAD MicReD unit

ABSTRACT

THE ELECTRICAL, thermal and optical parameters determining light emitting didoes (LEDs) operation are in a strong, mutual dependence; without knowledge about the parameters in one of these domains the other characteristics cannot be measured correctly. The reliability, useful operating life time and luminous flux are determined by the junction temperature of the LED device. This temperature is directly proportional to the total junction-to-ambient thermal resistance of the heat-flow path of the LED application. A dominant component of this overall thermal resistance is the junction-to-case thermal resistance of the LED package which is one of the key data sheet entries among the electrical and light output properties of the device. Unfortunately, until recently, there has been no widely accepted standard or recommendation regarding the correct measurement of this thermal resistance. This article describes the most recent LED thermal testing standards published by JEDEC in 2012 together with the new transient method for the measurement of the junction-to-case thermal resistance of power semiconductor device packages with an exposed cooling surface – aimed at the correct measurement of LEDs' thermal metrics for publication in a data sheet.

1. INTRODUCTION

Standardization is a wide ranging topic for which one can discuss extensively on product performance and testing standards. Until recently, standardization for LED products was lacking in comparison with those for classical light sources. For example, referring to "100W/230V E27/Par38 lamp" meant the same incandescent, directional light source everywhere in the world, regardless of its manufacturer.

Despite standardized nomenclature regarding LEDs aimed at solid-state lighting applications [1], there is currently no official classification. LEDs can be classified by color, outline or by luminous intensity (general, high-brightness, ultra high brightness). The rapid evolution of power LEDs in terms of different forms and flavors of packages impedes the definition of such component-level product standards. On the other hand, for assembly or module level units there have been attempts to develop interchangeable products. One representative product concept is, for example, GE's Infusion series of LED modules. A similar, but generalized concept is promoted by the Zhaga consortium [2] formed by several hundred LED vendors and luminaire manufacturers. The consortium aims to resolve the problem of LED product interchangeability by defining different LED modules and LED light engines each with clear definitions regarding their so-called *electrical, mechanical and thermal interfaces*. The goal is to enable interchangeability of LED light sources made by different manufacturers. Book[1] of Zhaga specifications, already available to the general public, describes the generic concepts, terms and definitions used by Zhaga,

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Besides his academic and industrial activities he has been involved in various national and international research projects (e.g. EU FW7 Fast2Light, KÖZLED, EU FW7 NANOPACK and most recently the EU FW7 NANOTHERM). He is active in the international standardization work regarding LEDs: he is member of the JEDEC JC15, CIE TC2-63, TC2-64 and TC2-76 technical committees. His fields of interest include thermal transient testing of packaged power semiconductor devices, characterization of LEDs and OLEDs, electro-thermal simulation.

including thermal-related topics. Additional Zhaga specification books define particular interface details for different LED light engine types. So far Books 2 and 3 are available to the general public. Zhaga plans to publish further (Books 4 to 8) outside the consortium at a later time. Though Zhaga have their own test specifications, none of the Zhaga books defines how to test thermal or thermal related properties of LEDs or LED products. The main focus is on determining the compliance to the different interface specs (electrical, mechanical, photometric, thermal) of Zhaga.

Thermal issues of LEDs are of paramount importance due to two reasons. On one hand, long-term reliability strongly depends on the operating junction temperature of the LEDs as most of the failure mechanisms leading to light output degradation are thermally assisted. Statistically seen this means that the so called "lumen maintenance" (precisely: long term maintenance of the emitted total luminous flux) of LED components is determined by the junction temperature: at higher junction temperature light output degradation happens more quickly. This is nicely illustrated by the so called Bxx-Lyy diagrams such as the B50-L70 plots usual in product data sheets. Such plots (see e.g. Figure 2 in [3]) present the expected life time of a power LED product as function of its junction temperature and forward current in terms of drop of its luminous flux to the 70% of the initial value (L70) in case of 50% of the investigated LED population (B50) – this being defined as failure condition (B50-L70).

On the other hand, the light output characteristics of LEDs strongly depend on the operating conditions. The forward current applied to an LED is the key variable; the higher the supplied current, the more light that is generated by the device. But the LED's light output drops when its junction temperature increases, even when the device is driven by a constant current source. This is illustrated in Figure 1. Both the intensity and the color output of an LED suffer when heat builds up. In Figure 1, the shift in the peak wavelength is evidence of a color change in the emitted light. Clearly this is not acceptable within an array of LEDs expected to produce homogeneous color over a large area, or when color stability is a strict requirement like in case of traffic lights.

Both examples highlight the importance of the junction temperature, but as observed in Figure 1, the forward current is also a key parameter. In fact, LEDs' operation extends to multiple domains: to electrical, thermal and optical, with rather strong mutual dependence among the major characteristic quantities like forward current, forward voltage, total light output (e.g. total radiant flux), heat generated within the device and the junction temperature, as illustrated in Figure 2. Therefore testing of power LEDs, including thermal characterization, is not straightforward. As the measurement of light emission of LEDs and LED-based products is affected by the junction temperature, CIE (International Commission on Illumination) have also revised their recommendations on LED measurements and established several technical committees (such as CIE TC2-64, TC2-64 or TC2-76) which aim to define LED testing procedures with consideration of LED operating junction temperature.

Thermal testing of LED components, or small LED as-

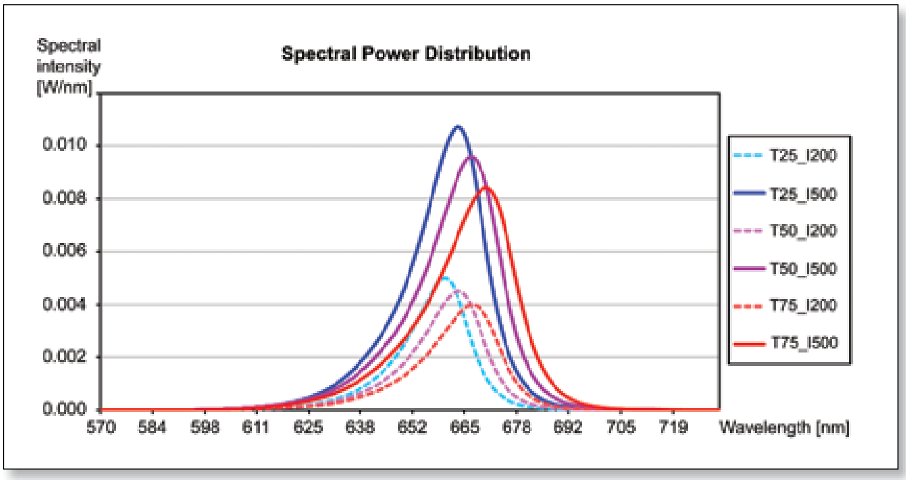

FIGURE 1: Current and temperature dependence of the spectral power distribution of the light output of a red LED. Plot labels indicate the temperature and current in the format Txx (°C)_Iyyy (mA). (Image courtesy of the Budapest University of Technology and Economics, Department of Electron Devices.)

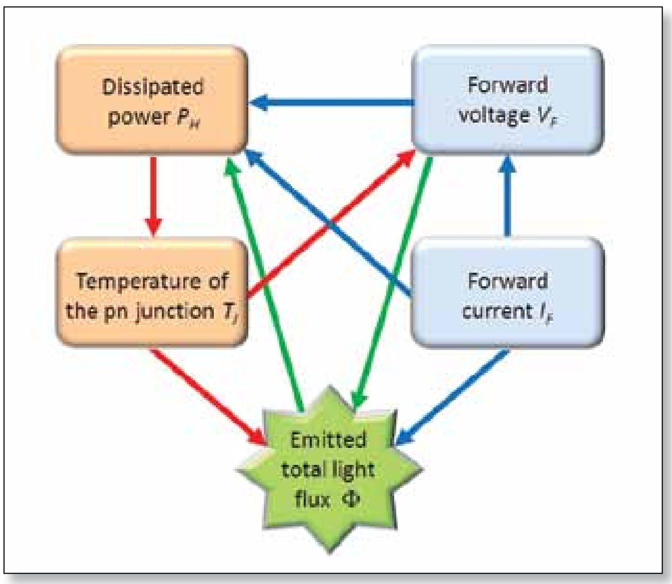

FIGURE 2: Mutual dependence of LEDs' major operating parameters.

[1] Zhaga call their distinct specification documents as books - this term is maintained in this article.

semblies, falls within the general category of thermal testing of packaged semiconductor devices – therefore the JC15 committee of JEDEC (Joint Electron Devices Engineering Council), dealing with on thermal characterization of packaged semiconductor devices initiated a series of white papers on the need for LED thermal testing standards (see e.g. [3]).

Based on the above discussions, the objective of this article is to provide an overview on results of the last five years' work of the JC15 committee by introducing the major concepts of LED thermal testing and providing a brief description of JEDEC's published standards of thermal testing of LED components [4], [5] , [6], [7] (LED packages or LED assemblies).

The JEDEC JC15 committee also deals with (compact) thermal modeling of semiconductor device packages aimed at board and system level thermal simulations. Such models are common for electrical components but due to the complex behavior of LEDs (see Figure 2) there are no standardized LED compact models yet which cover this multi-domain operation. This field is still the subject of additional research and future standardization. For an overview of the current state of the art on LED compact modeling the interested reader is advised to refer to the relevant section of a recent book on thermal management of LED applications [8].

2. HOW TO MEASURE THE REAL THERMAL IMPEDANCE AND THERMAL RESISTANCE OF LED PACKAGES?

2.1. The new JEDEC test procedure for obtaining junction-to-case thermal resistance of power semiconductor device packages

From the thermal point of view packaged LEDs are similar to any other power semiconductor device for which the most important thermal metric is their junction-to-case thermal resistance. For the accurate and repeatable measurement of this metric, the JEDEC JC15 committee has developed the new JESD51-14 testing standard [9] based on the so called *transient dual interface method*. This method is characterized as follows:

During the measurement it is assumed that there is a single heat conduction path from the junction (location of heating) towards the ambient through an exposed cooling surface of the package. This surface is called the package 'case'. A further assumption is that such packages are designed to be heat-sunk during normal operation. Thus, during a JESD 51-14 compliant R_{thJC} measurement the device under test needs to be attached to a cold plate. According to this standard the junction temperature cooling transients of the device need to be recorded twice, using the JESD 51-1 electrical test method [10], with two different qualities of the thermal interface between the package 'case' surface and the cold plate. In one measurement good thermal contact between the package 'case' and the cold plate need to be established (typically by applying a thermal interface material between the mating surfaces). This is also known as 'wet' condition as using a simple silicon oil wetting the interface is sufficient. In the other measurement poor thermal contact between the package and the test environment is required; that is no thermal interface material shall be used during this measurement. This condition is also known as 'dry' condition as no wetting material such ase silicon oil or thermal grease is used.

The effect of these two different qualities of the 'case' and 'cold plate' thermal interface on the two measured thermal impedance curves is that at a characteristic time the curves start diverging. The R_{th} value corresponding to this divergence point is the *transient junction-to-case thermal resistance*. The JESD 51-14 standard provides two methods to determine the 'exact' value of the transient R_{thJC} value in a repeatable and reproducible way. One method is based on the difference between the *structure functions*[2] .

The divergence point appearing in the structure function plots showing the results of the two measurements (with TIM and with no TIM) gives the exact value of the R_{thJC} junction-to-case thermal resistance of the package. According to the JESD 51-14 standard if the difference between the structure functions is greater than a pre-defined mismatch value, the divergence point is found. (The second method of finding the divergence point of the two measured thermal impedances defined in the standard is based on the difference of the first derivatives of these impedance curves – the divergence point and the corresponding R_{thJC} value is found in a similar way as in case of the structure function based method.)

More details on test method for JESD 51-14 are given by Schweitzer [11]. Müller et al [12] has published the first report on using this test method for the measurement of LEDs.

2.2. Measurement of the real thermal resistance / thermal impedance of LEDs

A semiconductor device package is typically characterized by a thermal resistance value specific for a given reference environment. According to the classical, almost-two-decades-old JESD 51-1 standard [10] the definition of the R_{thJ-X} *junction-to-reference environment X thermal resistance* is:

$$\textbf{1)}\quad R_{thJ\text{-}X} = \frac{T_J - T_X}{P_H}$$

where T_J denotes the *junction temperature*, T_X is the temperature of the reference environment X, P_H is the power dissipated at the the junction, i.e. the *heating power*. The R_{thJC} junction-to-case thermal resistance discussed in the previous section is such a characteristic thermal metric.

In case of a silicon diode the heating power is the product of the voltage drop across the diode and the current flowing through the pn-junction. Considering the high energy con-

[2] Structure functions are the thermal capacitance – thermal resistance maps of the junction-to-ambient heat-flow path; the shape of the structure function depends on the thermal properties and the geometry of the subsequent sections of the heat-flow path. For details on structure functions see the original papers of V. Székely or consult Annex A of the JESD 51-14 standard [9] or see Sections 4.4.4 and 4.4.5 of chapter 4 in [8].

version efficiency of today's power LEDs (in case of high end products close to 50%), during the calculation of the heating power one needs to consider the emitted optical power of the LED, the so called *total radiant flux* as well:

2) $P_H = I_F \cdot V_F - \mathbf{\Phi}_e$

where I_F and V_F denote the LED's forward current and forward voltage respectively, and $\mathbf{\Phi}_e$ is the power of the emitted light, the radiant flux (also known as *optical power* and denoted by P_{opt}). The accurate measurement of the total radiant flux is very important especially since it strongly depends on the junction temperature and on the LED's forward current (see Figure 2).

Thus, if the heating power is calculated according to Equation (2) during the JEDEC JESD 51-14 compliant transient junction-to-case thermal resistance measurements, the identified R_{thJC} value will be the *real, physical thermal resistance* of the LED package; so this value (or the approximate RC Cauer-type ladder model with a total cumulative thermal resistance equal to this value) can be used for compact thermal modeling of the LED package. Regarding the evolving topic of LED compact modeling the reader is advised to refer to section 6.5.2. of chapter 6 in [8].

When identifying the thermal resistance according to Equation (1) the junction temperature is measured indirectly taking advantage of the fact that in case of forced, constant forward current the forward voltage of any pn-junction almost linearly depends on the junction temperature. This is called the *electrical test method*; most commercial test equipment are based on this principle. The temperature dependence of the forward voltage is identified with the so called *K-factor calibration*. According to the classical thermal testing standards the T_X reference temperature also needs to be measured – this is typically done by using a thermocouple. The thermocouple also has to be calibrated. Thus, a disadvantage of the thermal resistance measurements based on Equation (1) is that two kinds of temperature sensors have to be calibrated: both the pn-junction and the thermocouple. From Equation (1) the junction temperature for two different values of the heating power (see also Figure 3b) can be expressed as:

3a) $T_{J1} = R_{thJ\text{-}X} \cdot P_{H1} + T_x$

3b) $T_{J2} = R_{thJ\text{-}X} \cdot P_{H2} + T_x$

Subtracting Eq. (3b) from Eq. (3a) the T_X reference temperature cancels out: $\Delta T_J = R_{thJ\text{-}x} - \Delta P_H$, thus

4) $R_{thJ\text{-}X} = \dfrac{\Delta T_J}{\Delta P_H}$

where $\Delta T_J = T_{J1} - T_{J2}$ and $\Delta P_H = P_{H1} - P_{H2}$, as illustrated in Figure 3b. This can be interpreted as follows. First a large I_H *heating current* (nowadays in the range of 350 mA to 1500 mA) is forced to the pn-junction of the LED. When at this current the junction temperature of the LED stabilizes (i.e. the forward voltage does not change any longer) one can measure the light output properties of the LED, including the $\mathbf{\Phi}_e = P_{opt}$ total radiant flux (emitted optical power) This measurement can be realized in an integrating sphere, following the recommendations of the CIE 127-2007 standard [13]. Knowing the forward current (I_H) and the forward voltage developing at this forced current across the pn-junction (V_H) and the $\mathbf{\Phi}_e = P_{opt}$ total radiant flux the P_{H1} power which heated the LED's pn-junction to the T_{J1} temperature can be calculated – see Figure 3a. After completing all optical measurements in the stable, hot state of the LED's pn-junction the I_H heating current is suddenly switched to a small I_M *measurement current*. (e.g. 10 mA). The heating power will be P_{H2}. When calculating this power, one can neglect the emitted optical power. At this very small, almost constant zero power the junction temperature will stabilize at the T_{J2} value after the cooling transient is completed. If the LED under test is attached to a cold plate (as also recommended by the JESD 51-14 standard), this transition typically takes approximately 30.120 sec. Dividing the measured $\Delta T_J(t) = T_{J1} - T_{J2}(t)$ junction temperature transient with the applied ΔP_H heating power step one obtains the *real* $Z_{th}(t)$ thermal impedance curve of the LED:

5) $Z_{th}(t) = \dfrac{\Delta T_J(t)}{\Delta P_H}$

The thermal resistance is the steady-

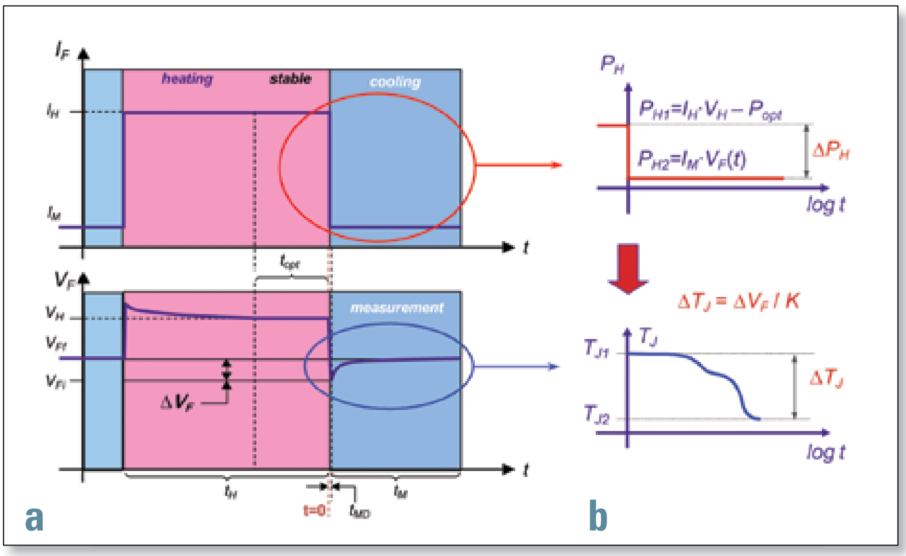

FIGURE 3: Waveforms during the thermal transient measurements of a power LED: **a)** forward current and forward voltage waveforms, **b)** heating power and junction temperature waveforms after switching the forward current from the I_H heating current to the I_M measurement current

state value of the thermal impedance:

$$\textbf{5)}\quad R_{thJ\text{-}X} = \frac{T_J(0)\text{-}T_J(\infty)}{P_{H1}\text{-}P_{H2}}$$

In practice $P_{H2} \cong 0$, therefore $T_J(\infty) = T_X$, thus classical definition of the thermal resistance provided by Equation (1) applies. Note, that with Equation (5) a new definition for the measurement of the thermal resistance is based on a differential approach. This approach has also been recommended by the JESD 51-14 standard for the transient method based R_{thJC} measurements.

Figure 4 presents the transient processes shown in Figure 3 in the I-V characteristic. Switching the forward current suddenly from the I_H heating current to the small I_M measurement current the forward voltage would jump from the V_H value to V_{Fi} – this later value will be the initial value of the forward voltage at the beginning of the cooling process. The change of the electrical operating point of the hot device from (V_H, I_H) to (V_{Fi}, I_M) takes a finite period of time (determined by the electrical capacitances of the *DUT & test equipment* setup). During this t_{MD} so called *measurement delay time* (indicated in Figure 3) there is a parasitic electrical transient, thus the data acquisition of the $\Delta V_F(t)$ junction temperature transient induced forward voltage change at the constant I_M measurement current has to be delayed. In practice the collected data points of the measured forward voltage transient corresponding to this parasitic electrical transient need to be discarded. The JEDEC JESD 51-14 standard [9] provides recommendations on how to separate the parasitic electrical transient from the real cooling transient and how to back extrapolate the missing part of the measured junction temperature transient to time $t = 0$. The implementation of the process is provided by a demo software tool forming an on-line Annex of the standard and is also available in professional, commercial implementations from thermal test equipment vendors.

What is specific to LEDs in the measurement process is the period marked as "stable" in Figure 3. This is an interval with a length appropriate for optical testing to measure the light output properties (including the radiant flux) of the test LED under steady state conditions as the LED light output measurement guidelines defined in the CIE 127-2007 standard [13] require. The summary of the complete measurement process required for the measurement of the real thermal resistance of power LEDs is provided in Figure 5.

2.3. The new LED thermal testing standards

As discussed in the previous sections, measurement of the emitted optical power is vital when calculating the LEDs' real thermal resistance (or thermal impedance if the dynamic thermal behavior is of interest). By neglecting the emitted optical power in this calculation the resulting thermal resistance / impedance value would be smaller – providing such (from marketing point of view more attractive) thermal metrics on LED data sheets can easily mislead customers and

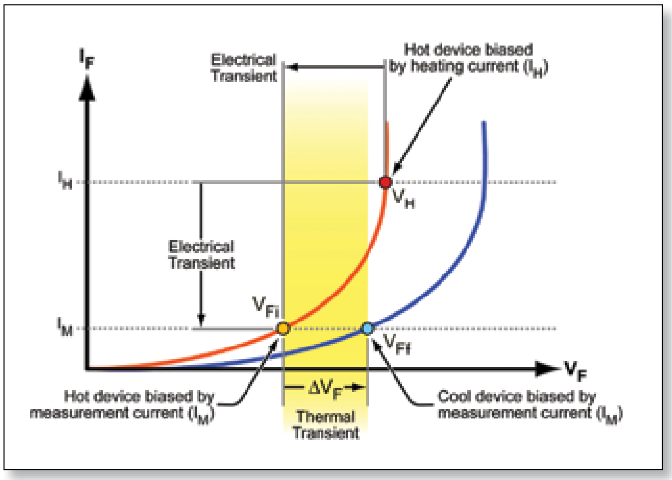

FIGURE 4: The transient processes shown in the I-V characteristic of an LED when its thermal properties are measured with the electrical test method

may result in improper design of the thermal management of the final LED application. This was the main motivation of the JEDEC JC15 committee when the work towards the definition of LED thermal testing standards commenced in 2008. Four standards have been worked out with the aim of fitting into the JESD 51-xx series of documents widely used in thermal characterization of packaged semiconductor devices. For LEDs the JESD 51-5x series of documents were published and April and May of 2012 and are summarized as follows:

- **JESD 51-50:** An overview document [4] that outlines the basic principles and possible future aspects of LED thermal characterization (including both testing and modeling). The document contains an overview chart which refers to the already published LED thermal characterization standards and includes foreseen topics of future standardization activities.
- **JESD 51-51:** This document [5] is the extension of the classical JESD51-1 standard [10] to the measurement of the real thermal resistance or real thermal impedance of power LEDs. When this standard is used in combination with the JESD 51-14 standard [9] (discussed in section 2.1), one can obtain the real junction-to-case thermal resistance of an LED package.
- **JESD 51-52:** This document [6] provides guidelines on how to apply the recommendations of the CIE 127-2007 standard regarding the measurement of the total flux of LEDs when such measurements are performed in combination with thermal testing of LEDs for the determination of the total radiant flux (emitted optical power). This JEDEC document also provides additional guidelines which were missing from the above CIE document.
- **JESD 51-53:** This document [7] is the glossary of terms and symbols used in the JESD 51-50 and 51-52 documents.

These new standards are essentially collections of definitions and additional recommendations / guidelines to prior standards such as JESD 51-1, JESD 51-14 and CIE 127-2007 which are needed for the correct thermal measurements of power LEDs. These additions are:

- It is recommended to use the R_{thJC} junction-to-case thermal resistance measured in a JESD 51-14 compliant way to characterize power LED packages.
- In accordance with the JESD 51-14 standard it is recommended to measure power LED components attached to a cold plate.
- Since the energy conversion efficiency may strongly depend on temperature, it is recommended to use such a thermal testing procedure in which the measurement results are not significantly affected by this. Therefore the JESD 51-51 standard recommends measuring the cooling transient of the junction temperature (like it is also recommended in the JESD 51-14 standard). To assure reproducibility of the measurement results it is recommended to report the set temperature of the test environment (cold plate).
- In the heating power the measured Φ_e total radiant flux (also known as P_{opt} emitted optical power) has to be considered – see Equation (2). This needs to be measured in a CIE 127-2007 compliant total flux measurement setup in such a way, that the test LED must be attached to the same temperature controlled cold plate as during the thermal test. It must be also assured that the "test LED – cold plate" remains intact between the thermal and optical measurements. In order to assure the consistency between the measured light output properties (total radiant flux, total luminous flux, color coordinates, etc) and the measured thermal metrics, it is recommended that during the total flux measurements the cold plate temperature is set to the same value as it was set for the thermal measurements.
- It is recommended to perform the thermal and radiometric/ photometric measurements in a single, combined setup (such as shown in Figure 5).
- When reporting the test results, besides the identified R_{thJA_real} real junction-to-ambient (i.e. junction-to-cold plate) thermal resistance, the T_{ref} reference temperature (cold plate temperature) and the T_J junction temperature calculated from these parameters with the following equation:

6) $T_J = T_{ref} + P_H \cdot R_{thJA\_real}$

The reported test results should also include the measured emitted optical power and the energy conversion efficiency. It is also advised to report the (junction) temperature dependence of the measured light output properties, both by means of plots and numerical tables.

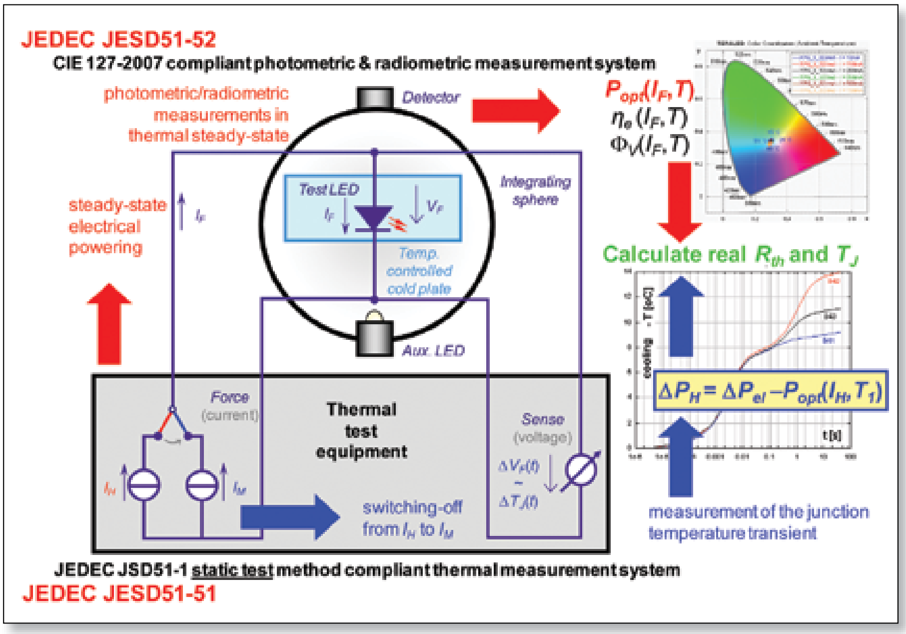

FIGURE 5: Combined thermal and radiometric / photometric test setup aimed at comprehensive testing of high power / high brightness LEDs, including measurement of the LEDs' real thermal resistance or thermal impedance and their real junction temperature

The scope of the JESD 51-51 and 51-52 standards is restricted to DC current-driven LEDs emitting light in the visible range. Measurement of the directly AC mains driven LEDs has specific issues. For an overview of these issues (which are being dealt with in the relevant technical committees such as JEDEC JC15, CIE TC 2-76) refer to e.g. section 4.7 of chapter 4 in [8].

3. CONCLUSIONS

In this article the concepts of the new JEDEC thermal testing standards relevant to LED thermal characterization have been introduced. These are the JESD 51-14 standard defining the so called transient dual interface method (TDIM) for the measurement of the junction-to-case thermal resistance of power semiconductor device packages with a single heat-flow path. This class of packages also includes most of the LED packages. The other set of standards is the JESD 51-5x series of standards, developed specifically for the correct thermal characterization of LEDs. The test setup suggested by these LED thermal testing standards is based on existing standards – the JESD 51-5x series of standards recommend to use a JESD 51-1 compliant thermal testing setup combined with a CIE 127-2007 compliant LED total flux measurement setup in order to account for the emitted optical power of LEDs during their thermal measurements. In such a setup the DC powering for both the thermal and optical test is provided by the thermal test equipment. The test LED should be attached to a temperature-controlled cold plate. This ensures reproducible thermal and light output measurements of LEDs.

The JEDEC LED thermal testing standards also include recommendations about data reporting. This is of key importance in order to assure that future LED product data sheets include information relevant for sufficient thermal design of the final LED application.

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Continued from page 2

In spite of this, extensive parametric analyses will be presented. In many instances, the findings – either experimental or numerical - remain essentially case-dependent, rather than sufficiently generic to permit the derivation of design rules, contrary to efforts in the 1980's and 1990's. But perhaps the most concerning is that too few conference papers today undertake a basic literature review to establish the originality of the work.

As a result, one now essentially refers to high quartile ranked journals for archival material, with conferences merely serving as a forum for keeping up-to-date with "who is doing what." No doubt that this critique may be controversial, but we all bear a responsibility when we either submit or review a conference paper to maintain standards that will ultimately best serve the electronic cooling community in the long term. Like many other conference organizing committee members, I often question where the line should be drawn between rigor and "giving the benefit of the doubt" to the authors. Since article acceptance/rejection decisions are rarely individually made, should conference organizing committees re-evaluate their objectives and organizing practices in the long term interest of the community? Given the current economic environment, will companies continue sending employees to conferences that do not enforce sufficient standards?

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